IN THE SPECIFICATION

Please replace the paragraph beginning at page 5, line 11, to page 6, line 9, with the following new paragraph:

A semiconductor memory device according to an aspect of the present invention includes, a plurality of word lines formed along a first direction; a plurality of bit lines formed along a second direction crossing at right angles to the first direction; a first memory cell including a magneto-resistive element which has either a first resistance or a second resistance smaller than the first resistance; a second memory cell including a magneto-resistive element which has a resistance between the first and second resistances; a memory cell array including the first and second memory cells disposed at intersections of a word line and bit lines; a row decoder which selects the word line; a row driver including a first current source that supplies a first write current to the word line selected by the row decoder and a second current source that supplies a second write current to the word line selected by the row decoder, an absolute value of the second write current being smaller than that of the first write current, the first current source supplying the first write current to the word line such that the magneto-resistive element of the first memory cell has either the first or second resistance to perform a write operation, and the second current source supplying the second write current to the word line such that the magneto-resistive element of the second memory cell has a resistance between the first and second resistances; a column decoder which selects a bit line; a column driver which supplies a third write current to the bit line selected by the column decoder; and a sense amplifier which amplifies data read from the first memory cell selected by the row decoder and column decoder.

Please replace the paragraph at page 6, lines 10-27, with the following new paragraph:

A control method of a semiconductor memory device according to another aspect of

the present invention includes, writing first data in a memory cell including a first magneto-resistive element, and writing second data in a reference cell including a second magneto-resistive element, the first magneto-resistive element of the memory cell in which the first data is written having either a first resistance or a second resistance smaller than the first resistance, the second magneto-resistive element of the reference cell in which the second data is written having a resistance between the first and second resistances; precharging a bit line; reading the first and second data in the bit line from the memory cell and reference cell; and amplifying the first data read in the bit line based on the second data. The memory cell and reference cell are disposed at an intersection of the bit line and word lines crossing at right angles to the bit line, and an absolute value of the write current supplied to the bit line and word line in writing the second data in the reference cell is smaller than that of the write current supplied to the bit line and word line in reversing the data held in the memory cell to write the first data in the memory cell.